TITLE **25G SFP28 DWDM 10km Transceiver**	**DOC No. RFD-20230815007-002**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
	DATE：2023.08.16	**CLASSIFICATION：Optics Transceiver**

1. SCOPE

The laser based 25Gigabit SFP28 Transceiver is designed to transmit and receive serial optical data over single mode optical fiber with 10Km.
They are compliant with SFF-8431,SFF-8432. The transmitter converts serial CML electrical data into serial optical data. The receiver converts serial optical data into serial CML electrical data.Digital diagnostics functions are available via a 2-wire serial interface, as specified in SFF-8472.

2. Product Features

- Compliant to SFP28 MSA
- Fully RoHS Compliant
- All metal housing for superior EMI performance
- Operating data rate up to 25.78Gbps
- High sensitivity APD photodiode and TIA
- LC duplex connector
- Hot pluggable 20pin connector
- Low power consumption <2 .3W
- -40℃ to 85℃ operating wide temperature range
- Single +3.3V±5% power supply
- Digital Monitoring SFF-8472 Rev 12.3 compliant

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3. PRODUCT DESCRIPTION

3.1 PRODUCT NAME

SFP28 25G DWDM Transceiver

Data Rate	Wavelength (nm)	Distance	Media	Power (dBm)	Sen. (dBm)	Connector	Temp.
25G	xxxxnm	10 km	SMF	-5~0	-19	LC	C
25G	xxxxnm	10 km	SMF	-5~0	-19	LC	I

Notes: Refer to the following table for wavelength.

Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C17 (1563.86nm)	C18 (1563.05nm)	C19 (1562.23nm)	C20 (1561.41nm)	C21 (1560.61nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C22 (1559.79nm)	C23 (1558.98nm)	C24 (1558.17nm)	C25 (1557.36nm)	C26 (1556.55nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C27 (1555.75nm)	C28 (1554.94nm)	C29 (1554.13nm)	C30 (1553.33nm)	C31 (1552.52nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C32 (1551.72nm)	C33 (1550.92nm)	C34 (1550.12nm)	C35 (1549.32nm)	C36 (1548.51nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C37 (1547.72nm)	C38 (1546.92nm)	C39 (1546.12nm)	C40 (1545.32nm)	C41 (1544.53nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C42 (1543.73nm)	C43 (1542.94nm)	C44 (1542.14nm)	C45 (1541.35nm)	C46 (1540.56nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C47 (1539.77nm)	C48 (1538.98nm)	C49 (1538.19nm)	C50 (1537.40nm)	C51 (1536.61nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C52 (1535.82nm)	C53 (1535.04nm)	C54 (1534.25nm)	C55 (1533.47nm)	C56 (1532.68nm)
Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)	Wavelength (nm)
C57 (1531.90nm)	C58 (1531.12nm)	C59 (1530.33nm)	C60 (1529.55nm)	C61 (1528.77nm)

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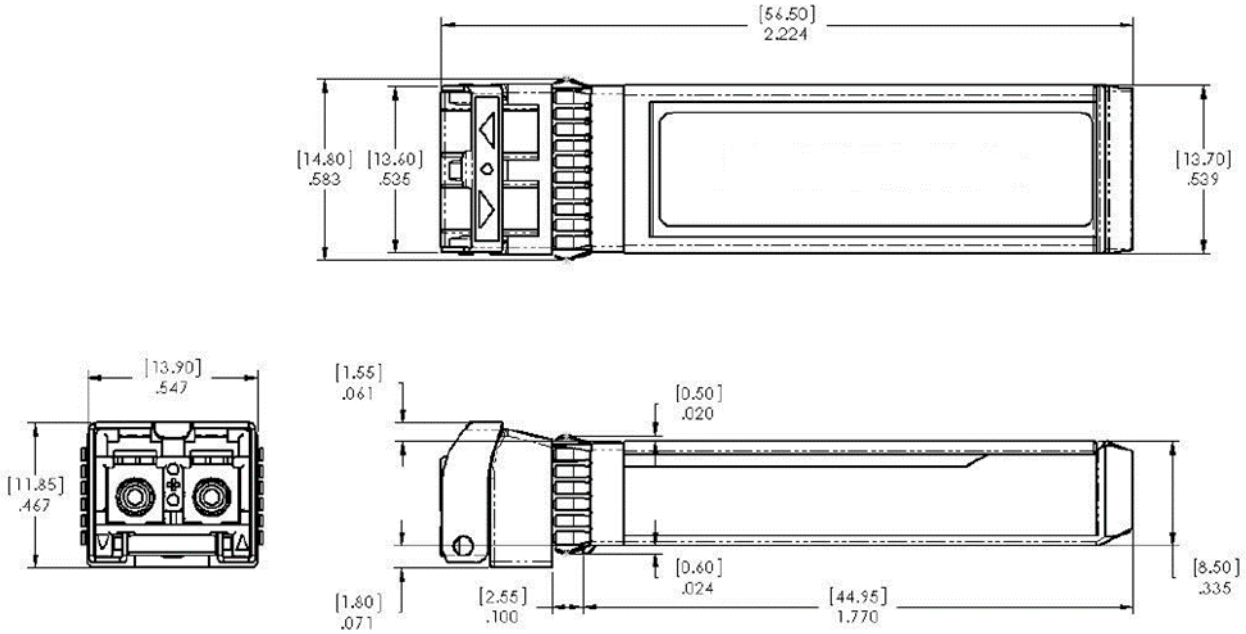
3.2 DIMENSIONS,MATERIALS,PLATINGS AND MARKING



Module Mechanical Dimensions

4. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 25G Ethernet
- CPRI Option 10

5. Absolute Maximum Ratings & Recommended Operating Conditions

Absolute Maximum Ratings				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Storage Temperature	TS	-40	+85	℃

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Maximum Supply Voltage	V_{CC3}	-0.5	4	V
Relative Humidity(Non-condensing)	RH	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature(I-temp)	TC	-40		85	℃
Power Supply Voltage	VCC	3.14	3.3	3.46	V
Bit Rate	BR			25.78	Gb/s
Transmission Distance	TD			10	Km
Bit Error Ratio	BER			$5*10^{-5}$	
Supply Curent	Icc			690	mA
Max Supported Link Length	L			15	km
Max Supported Link Length	L			80	km

Note1: Measured without DCM.

Note2:Measured with 80km DCM.

Transmitter Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Nominal Wavelength	λ	1528		1565	nm	
Center wavelength Spacing	GHz	-	100			
Average Optical Power	Pavg	0		5	dBm	
Extinction Ratio	ER	6	-	-	dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Laser Off Power	Poff	-	-	-30	dBm	-

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Input Differential Impedance	R_{IN}	80	100	120	Ω	
Differential Data Input	VIN	150		1200	mVp-p	-
Transmit Disable Voltage	V_{DIS}	2		V_{CCHOST}	V	
Transmit Enable Voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V	
Transmit Fault Assert Voltage	V_{FA}	2		V_{CCHOST}	V	
Transmit Fault De-Assert Voltage	V_{FDA}	V_{EE}		V_{EE}+0.4	V	

Receiver Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Center Wavelength	λc	1260		1620	nm	
Receiver Sensitivity(Averaged)	SEN			-19	dBm	1
ReceiverSensitivity(Averaged)@10km	SEN			-16	dBm	
Receiver Overload		-5	-		dBm	
LOS De-Assert	LOSD	-	-	-20	dBm	-
LOS Assert	LOSA	-30	-	-	dBm	-
LOS Hysteresis	-	0.5	-	5	dB	-
Optical Return Loss			-	-26	dB	
Differential Data Output	V_{OD}	350		700	mVp-p	
Output Rise Time	t_{RISE}	25			pS	
Output Fall Time	t_{FALL}	25			pS	
LOS Fault	V_{LOSFT}	2		V_{CCHOST}	V	
LOS Normal	V_{LOSNR}	V_{EE}		V_{EE}+0.4	V	

Note1: Measured at 12.5Gbps,ER>3.5dBm, PRBS 2^{31}-1 and BER better than or equal to 10E-12;

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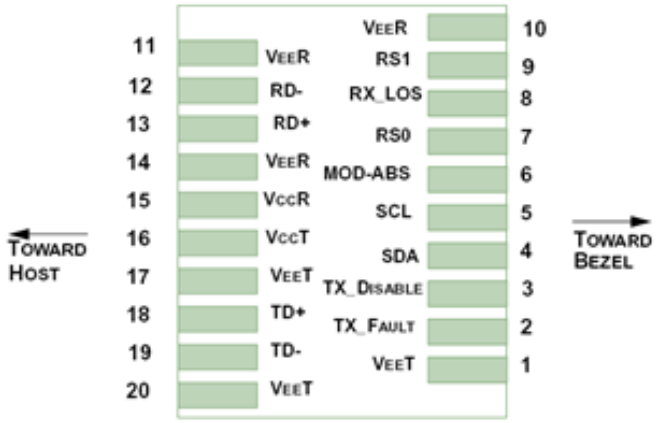
6. Pin-out Definition:



Pin Definitions

Pin Assignment

Pin Number	Symbol	Name	Description
1,17,20	VeeT	Transmitter Signal Ground	These pins should be connected to signal ground on the host board.
2	TX Fault	Transmitter Fault Out (OC)	Logic “1” Output = Laser Fault (Laser off before t_fault) Logic “0” Output = Normal Operation This pin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.
3	TX Disable	Transmitter Disable In (LVTTL)	Logic “1” Input (or no connection) = Laser off Logic “0” Input = Laser on This pin is internally pulled up to VccT with a 10 kΩ resistor.
4	SDA	Module Definition Identifiers	Serial ID with SFF 8472 Diagnostics Module Definition pins should be pulled up to Host Vcc with 10 kΩ resistors.
5	SCL		
6	MOD-ABS		

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7 9	RS0 RS1	Receiver Rate Select (LVTTL) Transmitter Rate Select (LVTTL)	These pins have an internal 30kΩ pull-down to ground. A signal on either of these pins will not affect module performance.
8	LOS	Loss of Signal Out (OC)	Sufficient optical signal for potential BER < $1x10^{-12}$ = Logic “0” Insufficient optical signal for potential BER < $1x10^{-12}$ = Logic “1” This pin is open collector compatible, and should be pulled up to Host Vcc with a 10kΩ resistor.
10,11,14	VeeR	Receiver Signal Ground	These pins should be connected to signal ground on the host board.
12	RD-	Receiver Negative DATA Out (CML)	Light on = Logic “0” Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
13	RD+	Receiver Positive DATA Out (CML)	Light on = Logic “1” Output Receiver DATA output is internally AC coupled and series terminated with a 50Ω resistor.
15	VccR	Receiver Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure 3.Recommended power supply filter
16	VccT	Transmitter Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Figure 3.Recommended power supply filter
18	TD+	Transmitter Positive DATA In (CML)	Logic “1” Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.
19	TD-	Transmitter Negative DATA In (CML)	Logic “0” Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100Ω resistor.

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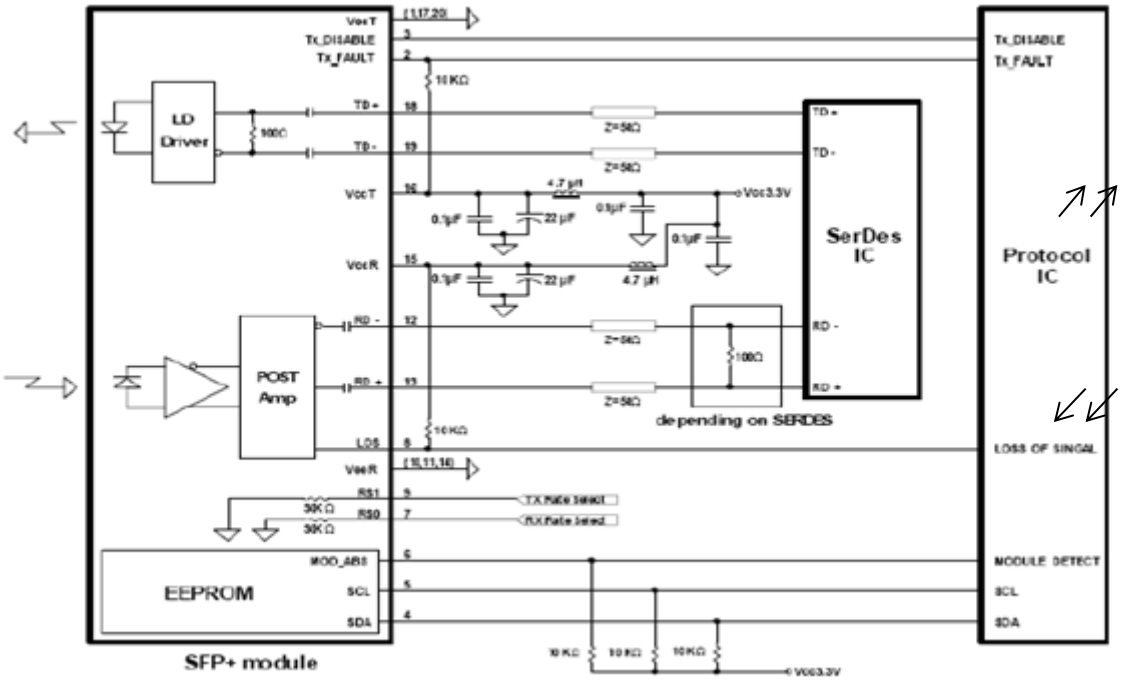
Recommended Interface Circuit



Typical application circuit

7. Digital Diagnostic Memory Map

As defined by the SFF-8472, Our SFP28 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

●Transceiver temperature

●Laser bias current

●Transmitted optical power

●Received optical power

●Transceiver supply voltage

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It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range. The operating and diagnostics information is monitored and reported by a DigitalDiagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessedthrough the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the SFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the SFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.For more detailed information, including memory map definitions, please see the SFF-8472 documentation1.

8.Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2023.08.16	Andy Yang	Mike Sun